Contact engineering for organic semiconductor devices via Fermi level depinning at the metal-organic interface

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(Received 11 March 2010; revised manuscript received 16 June 2010; published 20 July 2010)

Organic or carbon semiconductor devices are promising for both nanoelectronic and macroelectronic applications. One of the major challenges to achieve high performance of these devices lies on understanding and improving the metal-organic (M/O) interface. In this paper, we present evidence and demonstration of Fermi-level depinning at the M/O interface by inserting an ultrathin interfacial Si_3N_4 insulator in between. The M/O contact behavior is successfully tuned from rectifying to quasi-Ohmic and to tunneling by varying the Si_3N_4 thickness within 0–6 nm. Detailed physical mechanisms of Fermi-level pinning/depinning responsible for the M/O contact behavior are clarified based on a lumped-dipole model and a simple depinning model. This work sheds light on the fundamental understanding of the M/O interface properties and also proves a practical engineering method of achieving low-resistance quasi-Ohmic contacts for organic electronic devices.

DOI: 10.1103/PhysRevB.82.035311 PACS number(s): 73.40.−c, 73.61.Ph

I. INTRODUCTION

Organic (carbon) electronic materials such as graphene, carbon nanotube, small-molecule and polymer semiconductor, have been playing an increasingly important role in the emerging macroelectronic and nanoelectronic areas.[1–3] Of particular interest toward practical applications are organic solar cells, organic light-emitting diodes (OLED), as well as large-area flexible displays, sensors, and integrated circuits based on organic thin-film transistors.[1–6] Over the past decade, organic device performance has been significantly boosted by virtue of material synthesis, process optimization, and device engineering.

Despite the encouraging progress, many issues remain. One of the major challenges in achieving high performance of organic devices lies in their metal-organic (M/O) contacts. Previous work on both device modeling[7,8] and experimental study[9–13] has shown explicitly the critical role of M/O contacts in determining the device performance, including the electrical characteristics, the channel potential profile, and the extrinsic field-effect mobility. It is now well recognized that, in order to achieve optimized high-performance devices, one must lower the charge injection barrier height and minimize the localized trap states at the M/O interface.

Achieving this goal turns out to be an arduous task. Both theoretical[14–16] and experimental[17–19] studies reveal that a high Schottky injection barrier can emerge at the M/O interface irrespective of the metal work function, a phenomenon known as Fermi-level pinning, which gives rise to poor contact properties and unfavorable organic semiconductor device performance.

In this paper, we present evidence and demonstration of Fermi-level depinning at the M/O interfaces by inserting an ultrathin interfacial Si_3N_4 insulator in between.[20] The M/O contact behavior is successfully tuned from rectifying to quasi-Ohmic and to tunneling by varying the Si_3N_4 thickness within 0–6 nm. Detailed physical mechanisms of Fermi-level pinning/depinning responsible for the M/O contact behavior are clarified based on a lumped-dipole model and a simple depinning model. Experimental results are found in good agreement with the pinning/depinning theory and the proposed model.

II. EXPERIMENTAL RESULTS

We chose *p*- and *n*-type organic semiconductors, pentacene, and 3,4,9,10-perylene-tetracarboxylic-dianhydride (PTCDA), respectively, for this study. Both materials have been found to exhibit relatively strong Fermi-level pinning at their M/O interfaces,[21] with a pinning factor ($S = d\phi_b / d\psi_{metal}$) of $S \sim 0.4$ for metal/pentacene and $S \sim 0$ for metal/PTCDA. Si_3N_4 was chosen as the interfacial layer because (1) less-oxygen environment during the deposition process suppresses unintentional oxidation of the underlying organic materials, and (2) Si_3N_4 has a moderately large band gap with the conduction/valence band being relatively far away from the lowest unoccupied molecular orbital (LUMO)/highest occupied molecular orbital (HOMO) level of the aforementioned organic semiconductors, thus excluding the possibility of charge injection assisted by a close transition energy level as traditionally suggested for organic transistors, solar cells, or light-emitting diodes with an interfacial transition metal oxide layer.[22,23] For this work, Si_3N_4 layer with thickness of 0–6 nm (as measured on dummy silicon wafers by ellipsometry) was deposited at room temperature by a precisely controlled high-vacuum LSI sputtering system.

Figure 1(a) illustrates the device structure and the process flow for our Au/Si_3N_4/pentacene diodes. Atomic force microscope (AFM) characterization on the pentacene films as shown in Fig. 1(b) indicates that there is no damage caused by the Si_3N_4 sputtering process on the underlying organic semiconductor layer. A large Au electrode is used as the common anode, and the cathode electrodes with a much smaller area are either Au pads as deposited by thermal evaporation or Au bonding wires. We found that the diodes

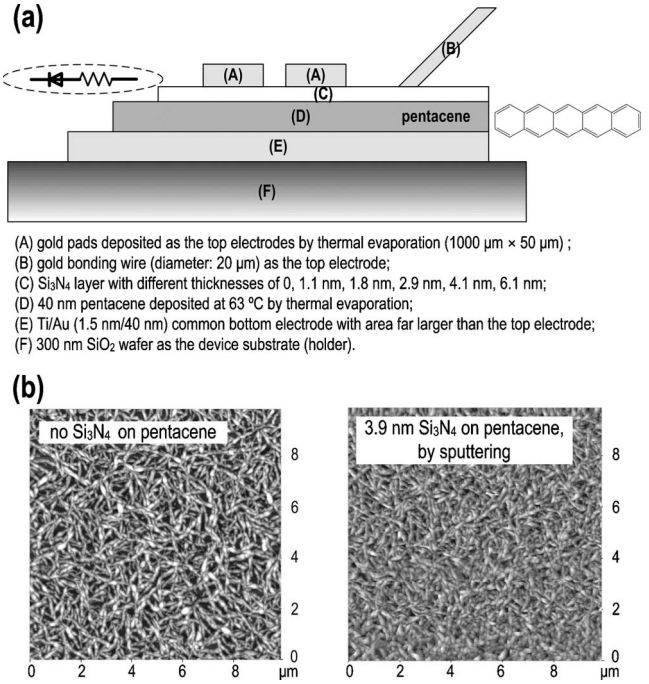


FIG. 1. (a) Device structure and process flow of the Au/Si_3N_4/pentacene diodes. Pentacene was chosen for this study since the pinning factor ($S=d\phi_b/d\psi_{metal}$) $S\sim 0.4$ is relatively small for the metal/pentacene interface. (b) AFM images of 200 nm pentacene films deposited on Au at room temperature before/after Si_3N_4 sputtering deposition. Height scale: 300 nm.

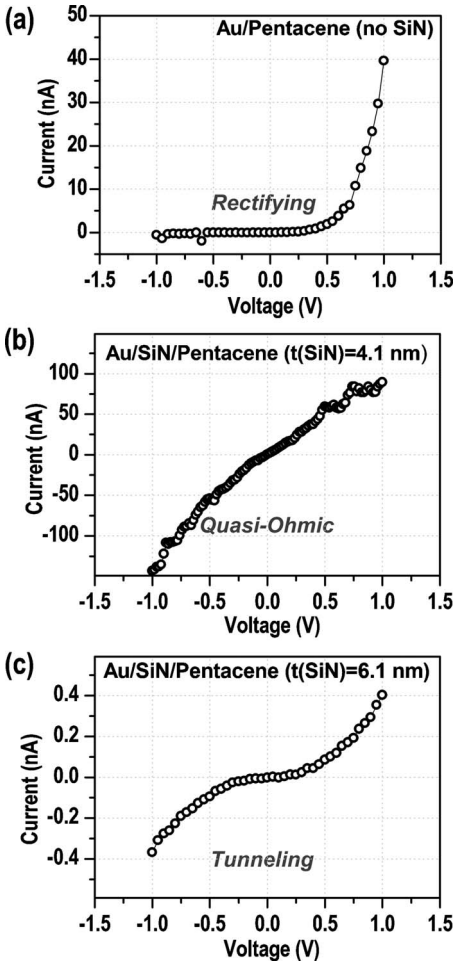


FIG. 2. *I-V* characteristics of the Au/Si_3N_4/pentacene diodes with different Si_3N_4 thicknesses (with Au wire as the top cathode electrode), providing direct evidence that the Au/pentacene diode has been successfully tuned to rectifying, quasi-Ohmic, and symmetric tunneling behavior by modulating the Si_3N_4 thickness. (Note: the effective contact area between the Au wire and the Si_3N_4/pentacene is only a fraction of the wire cross section due to the surface roughness of Si_3N_4/pentacene layer, and may vary from device to device. One should note that the *I-V* profile revealing the diode property is what really counts here.)

with/without Si_3N_4 based on the evaporated Au pads are consistently shorted due to Au atoms penetration, leading to an artifactual Ohmic contact with very low resistance.

To resolve the shorting issues and eliminate the electrical artifacts resulting from the gold atom penetration, we introduced the gold wire based diode configurations as depicted in Fig. 1(a) for this study. Figure 2 shows the measured *I-V* characteristics of the Au/Si_3N_4/pentacene diodes with different Si_3N_4 thicknesses, providing direct evidence that the metal-organic semiconductor diodes are successfully tuned from rectifying to quasi-Ohmic and to tunneling ones with increase of the Si_3N_4 thickness in between, in excellent agreement with the Fermi-level pinning/depinning theory and model as introduced in Sec. III. Quasi-Ohmic contact behavior for Au/pentacene is observed when the Si_3N_4 thickness is nominally ~4 nm. Figure 3 shows the normalized dynamic resistance ($R_{AC}=\partial V/\partial I$) and static resistance ($R_{DC}=V/I$) of the Au/Si_3N_4/pentacene diodes with respect to different Si_3N_4 thickness. Both resistances reach the minimum at an optimal Si_3N_4 thickness of ~4.1 nm, which further collaborates effective Fermi-level depinning and contact resistance reduction by the Si_3N_4 interfacial layer. At first glance it is surprising that a nominal Si_3N_4 thickness of ~4 nm leads to quasi-Ohmic contact (from the perspective of tunneling). After taking into account the surface roughness of the underlying organic layer, which lowers the effective Si_3N_4 thickness, we argue that such an experimental observation is still expectable, and, importantly, it is useful for practical applications.

We also fabricated Ag/Si_3N_4/PTCDA diode array as shown in Fig. 4 for this study. Instead of measuring an individual diode's *I-V* curve, here we evaluated the contact resistance of Ag/Si_3N_4/PTCDA by measuring two back-to-back diodes in series connection with a low-conductivity PTCDA bulk film [see Fig. 5(a)]. The concept is that the measured total resistance, R_{total}, can be described as

$$R_{total} = R_c + R_{film} = \frac{r_c}{W \cdot L} + \alpha \cdot R_{sh(film)} \frac{l}{L}, \qquad (1)$$

where r_c is the contact resistivity in terms of the product of contact resistance, R_c, and the contact area, $W \times L$, and it reflects the contact property of the Ag/Si_3N_4/PTCDA interface. R_{film} is the resistance of the low-conductivity PTCDA bulk film between the two interfaces, $R_{sh(film)}$ is the sheet resistance of the film, l is the film length, and α is a correction factor reflecting the current crowding effect from the

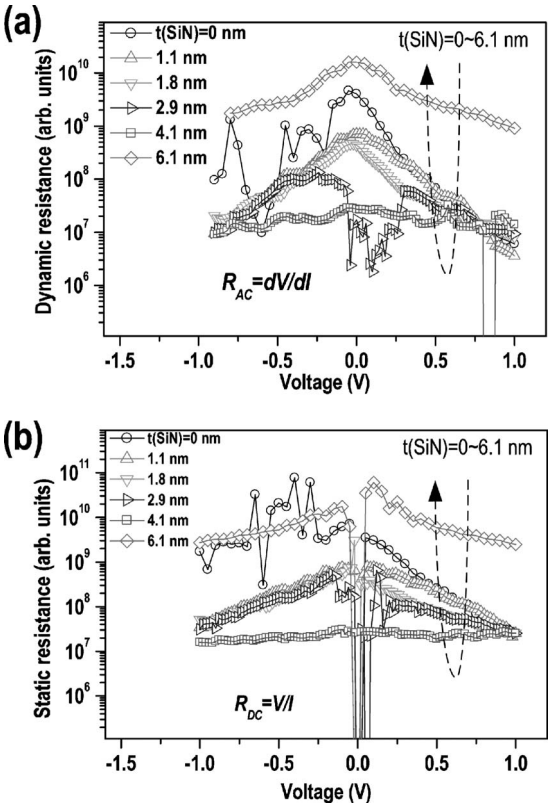
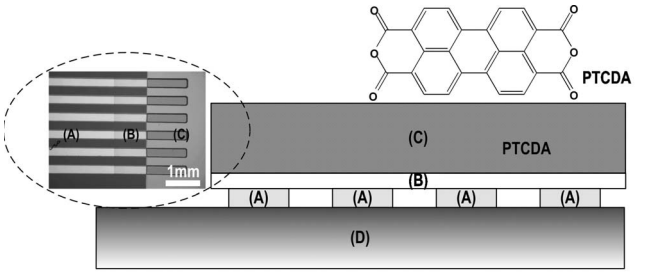


FIG. 3. Normalized dynamic resistance ($R_{AC}=\partial V/\partial I$) and static resistance ($R_{DC}=V/I$) of the Au/Si_3N_4/pentacene diodes with respect to the Si_3N_4 thickness, as calculated from their *I-V* measurement curves. Normalization is performed based on the fact that the maximum forward-biased diode current (here defined at $V=+1$ V) is less affected by the Si_3N_4 thickness. (Note: The device with a thick Si_3N_4 layer ($t=6.1$ nm) was not normalized since tunneling dominates therein.)

Ag/Si_3N_4/PTCDA interface to the film. Simple transformation of formula (1) yields

$$R_{\text{total}} \cdot W \cdot L = r_c + \alpha \cdot R_{\text{sh(film)}} \cdot l \cdot W \approx r_c + \text{const} \qquad (2)$$



(A) Ag electrode array with thickness=30 nm and spacing=250 μm acting as bottom electrodes;
(B) Si_3N_4 layer with different thicknesses of 0.6 nm, 1.0 nm, 1.9 nm, 2.4 nm, 3.2 nm, 3.9 nm, 6.1 nm;
(C) 130 nm PTCDA deposited at room temperature by thermal evaporation;
(D) 300 nm SiO_2 wafer as the device substrate (holder).

FIG. 4. Device structure, microscopy image, and process flow of the Ag/Si_3N_4/PTCDA diodes. PTCDA was chosen here since the pinning factor ($S=d\phi_b/d\psi_{\text{metal}}$) is $S\sim 0$ for metal/PTCDA interface, indicating very strong Fermi-level pinning effect at the metal/PTCDA interface.

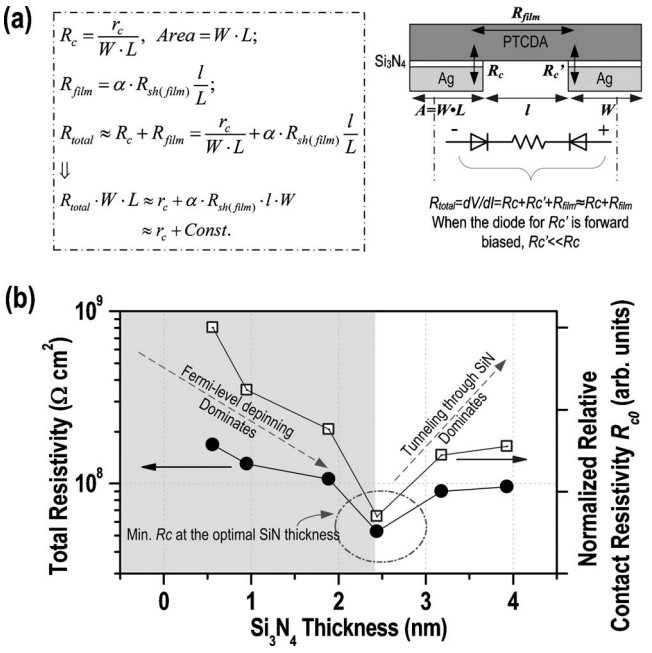


FIG. 5. (a) A quick and straightforward extraction method for the relative contact resistivity of the M/O interface with different Si_3N_4 thicknesses, by measuring the *I-V* characteristics on two adjacent electrodes; (b) A minimum contact resistivity is observed at the Ag/PTCDA interface with a sandwiched Si_3N_4 thickness of ~2.5 nm, reaffirming Fermi-level depinning at the M/O interface by inserting the ultrathin interfacial Si_3N_4 layer.

Therefore, by measuring the total resistance of the series connected diodes and the bulk film and taking into account the device size, we can directly extract the relative contact resistivity of the Ag/Si_3N_4/PTCDA interface. Figure 5(b) clearly shows a minimum contact resistivity is observed for the Ag/PTCDA interface with an optimal sandwiched Si_3N_4 thickness of ~2.5 nm, reaffirming the occurrence of Fermi-level depinning at M/O interface by inserting the ultrathin Si_3N_4 interfacial layer. The apparent difference of the optimal Si_3N_4 thickness for Au/pentacene and Ag/PTCDA interfaces can be attributed to their different interface roughness (and thus different effective interfacial layer thickness). This also underscores that one should consider the particular device structure and materials therein when applying the Fermi-level depinning technology to high performance organic devices.

III. THEORY AND PROPOSED MODEL

Intuitively, introducing an ultrathin Si_3N_4 layer between the metal-organic semiconductor interface gives rise to a few effects. One is the change of the organic film's localized states distribution close to the M/O interface,[6,24] because the Si_3N_4 layer protects the organic film from physical interference of the metal deposition in top-contact structure (see Fig. 1) and facilitates organic film growth on the metal in bottom-contact structure (see Fig. 4). Another effect is the modulation of the charge injection barrier height, ϕ_b. We now proceed to discuss the mechanism responsible for this effect, namely Fermi-level depinning effect.

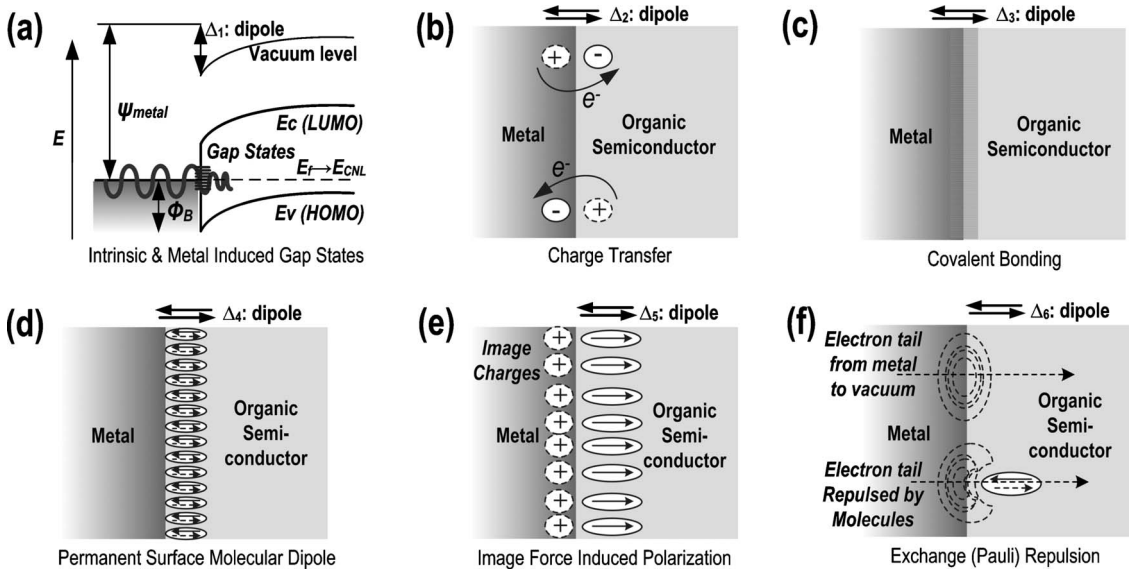


FIG. 6. Different mechanisms of Fermi-level pinning at the metal/organic semiconductor interface, including (a) MIGS and intrinsic surface states, (b) charge transfer, (c) covalent bonding, (d) permanent molecular dipole, (e) image force, and (f) exchange/Pauli repulsion. An interface dipole is always created upon the M/O junction formation.

Classical metal-induced gap states (MIGS) theory[25] has been applied to explain Fermi-level pinning/depinning at traditional metal-inorganic semiconductor (e.g., Si[26] or Ge[27]) interface. The concept is simply illustrated in Fig. 6(a): free-electron wave function penetrates into the semiconductor band gap, resulting in a large amount of MIGS which pin the Fermi energy close to the charge neutrality level (CNL) and form a large Schottky barrier for charge injection. However, the scenario for M/O interfaces is found more complicated, and a variety of mechanisms as shown in Figs. 6(a)–6(f) have been suggested to understand the M/O interfacial electronic structures.[18,19,21] The overall effect is an interface di-

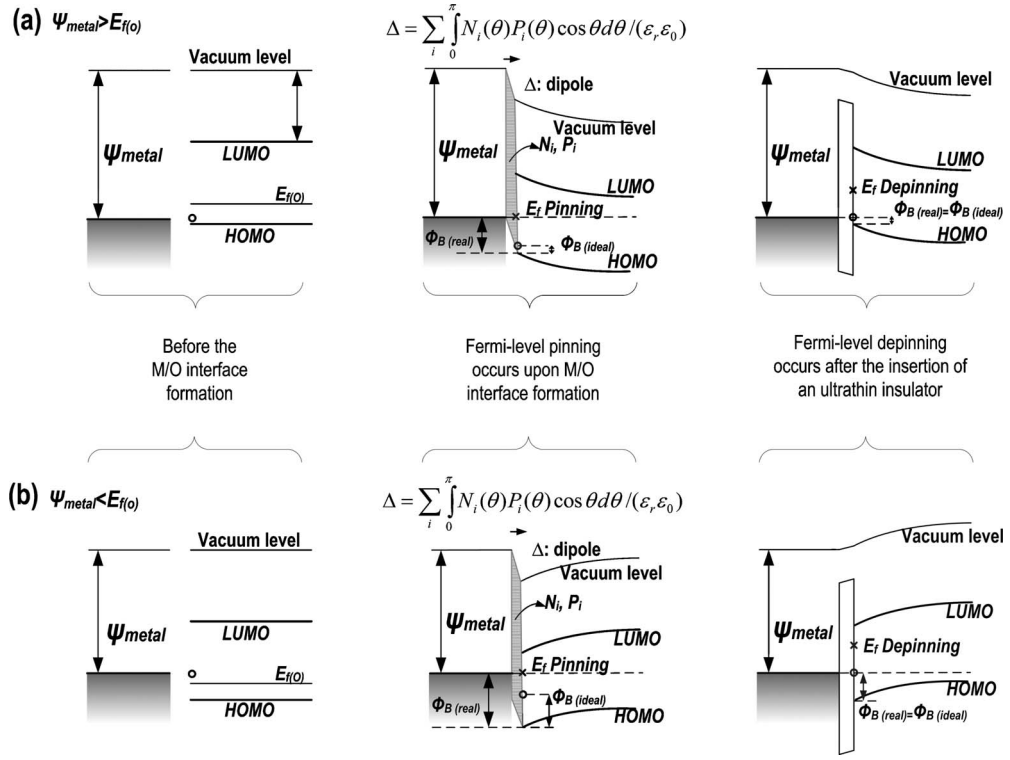


FIG. 7. M/O interface energy band diagrams under different circumstances: before M/O interface formation; upon M/O interface formation, Fermi-level pinning arises from various interface dipole elements; and after inserting an ultrathin Si_3N_4 insulator, the Fermi-level depinning takes effect by blocking the physisorption/chemisorption at the M/O interface. (a) and (b) corresponds to the case that the metal work function is larger and smaller than the organic semiconductor's Fermi energy level, respectively.

pole (Δ) created upon the formation of the M/O junction. Note that there can be disorder-induced energy level fluctuations and Anderson localized states at the M/O interface,[6,24] which are shown only leading to an effective barrier lowering by $\sigma^2/2kT$, where σ is the Gaussian energy distribution width of the localized states, k is the Boltzmann constant, and T is the temperature. For simplicity and clarity, effective HOMO/LUMO levels are denoted in this paper.

Figure 7 shows a generalized energy band diagram before and after the insertion of the Si_3N_4 insulator between the M/O interface, where (a) and (b) corresponds to the case of metal work function, ψ_{metal}, being larger and smaller than the p-type organic semiconductor's Fermi energy level, $E_{f(O)}$, respectively. When the M/O interface is created without any interlayer, MIGS, charge transfer, covalent bonding, permanent surface molecular dipole, image force-induced polarization, and Pauli repulsion as illustrated in Fig. 6 all contribute to a lumped interface dipole, of which the magnitude depends on the metal and thus automatically tunes. This gives rise to the apparent Fermi-level pinning within the organic semiconductor band gap and being further away from the carrier transport energy level, i.e., HOMO in Fig. 7. Therefore, the measured injection barrier height, $\phi_{b(\text{real})}$, can be considerably larger than the Schottky–Mott limit, $\phi_{b(\text{ideal})}$, due to the interface dipole induced energy shift Δ. This effect can be modeled by

$$\phi_{b(\text{real})} = \phi_{b(\text{ideal})} + \Delta = U[\text{HOMO} - \psi_{\text{metal}}] \cdot (\text{HOMO} - \psi_{\text{metal}}) + \sum_i \int_0^{\pi} \frac{N_i(\theta) \cdot P_i(\theta) \cdot \cos\theta}{\varepsilon_r \varepsilon_0} d\theta, \quad (3)$$

where $U[x]$ is the unit step function of x (i.e., $U[x]=0$ if $x<0$, and $U[x]=1$ if $x \geq 0$), θ is the alignment angle between the dipole element and the interface normal, N_i and P_i are, respectively, the density and moment of the dipole element type i, corresponding to different dipole origins as shown in Fig. 6. Since large charge injection barrier at the source/drain of organic thin-film transistors (TFT) leads to significant contact resistance which deteriorates the extrinsic electrical performance of the TFT, it is crucial to mitigate Fermi-level pinning effect at the M/O interfaces, and the dipole elements from all aforementioned mechanisms, N_i and P_i, should be eliminated. As illustrated in Fig. 7, an ideal insulator shields physisorption/chemisorption at the M/O interface and releases the Fermi level pinning. A quasizero Schottky barrier or Ohmic contact is thus anticipated under depinning circumstances.

To understand the Fermi-level depinning effect more quantitatively, we propose a simple depinning model based on the fact that there are two competing mechanisms responsible for the charge injection current or contact resistance after inserting the interfacial insulator. One is the direct or Fowler-Nordheim (FN) tunneling through the insulator with the charge carrier tunneling probability, $\gamma_{(\text{tunneling})}$, exponentially decreasing with the insulator thickness, t. The other mechanism is thermionic emission such as charge injection over the effective Schottky barrier, $\phi_{b(\text{real})}$, which decreases with the insulator thickness due to the Fermi-level depinning effect. The thermionic emission probability, $\gamma_{(\text{emission})}$, thus, increases with the insulator thickness. The overall charge carrier injection depends on both processes with its probability being proportional to $\gamma_{(\text{tunneling})} \times \gamma_{(\text{emission})}$. Therefore, the contact resistance can now be described as

$\Phi_{b(\text{ideal})}$ (eV)	Δ (eV)	t_c (nm)	β_1 (eV^{-1})	β_2 (nm^{-1})	n
0.5	0.5	2	5	0.35	2

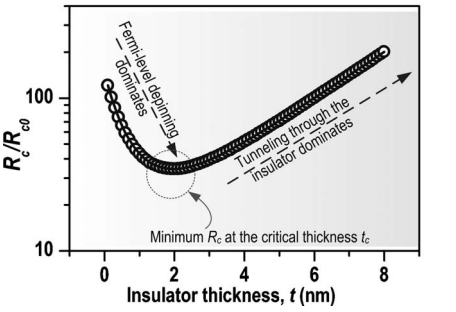


FIG. 8. Simulation plot of the contact resistance with respect to the interfacial insulator thickness at the M/O interface based on the proposed simple depinning model. All of the parameter values for Eqs. (4) and (5) are listed in the table. Here a critical insulator thickness of $t_c=2$ nm is used for this exemplified simulation purpose.

$$R_c \cong R_{c0} \cdot \exp(\beta_1 \cdot \phi_{b(\text{real})}) \cdot \exp(\beta_2 \cdot t), \quad (4)$$

where β_1 and β_2 are thermionic emission coefficient and tunneling coefficient, respectively, and R_{c0} is the contact resistance with vanished barrier height and no interfacial interlayer. Since the interlayer insulator hinders physisorption/chemisorption between the metal and the organic semiconductor, we assume roughly that the induced dipole moments, $N_i(\theta)P_i(\theta)$ in Eq. (3), decrease with the blocking layer thickness in a semi-empirical nonlinear exponential form. For simplicity, a lumped mathematical description is assumed to take into account all the effects described in Fig. 6 including the MIGS which is induced by the electron wave penetration. The measured barrier height thus follows

$$\phi_{b(\text{real})} = \phi_{b(\text{ideal})} + \Delta \cdot [\exp(-t/t_c)]^n \quad (5)$$

where $n>1$ is an exponent representing the insulator's blocking efficiency, and t_c is the critical thickness. Combine Eqs. (3)–(5), we are able to quantify how the contact resistance changes with the interlayer insulator thickness.

Figure 8 shows an exemplified simulation plot of the contact resistance with respect to the insulator thickness based on the above depinning model, which is in good agreement with our experimental results as discussed in Sec. II. We emphasize that the insulator thickness must be optimized carefully: initial increase of the insulator thickness reduces the contact resistance due to Schottky barrier modulation as a result of Fermi-level depinning effect; once beyond the optimal thickness, tunneling resistance through the insulator dominates rapidly.

IV. SUMMARY

We demonstrated Fermi-level depinning at two different M/O interfaces by inserting a precisely-controlled ultrathin

interfacial Si_3N_4 layer. The contact behavior is tuned from rectifying to quasi-Ohmic and to tunneling by modulating the Si_3N_4 thickness within 0–6 nm. We also presented a lumped-dipole model and a simple depinning model to clarify the detailed physical mechanisms of Fermi-level pinning/depinning effect at the M/O interface. Experimental results are in good agreement with the theory and the proposed model. This work represents an important step toward the fundamental understanding of M/O interface properties. In addition, it proves a feasible engineering method of achieving low-resistance quasi-Ohmic contacts for organic electronic devices, and can be particularly useful for the optimization of organic transistor performance through source/drain contact engineering.

ACKNOWLEDGMENTS

The authors would like to acknowledge Masaki Okajima for his helpful discussions and the funding support for this work from Toshiba Inc. through Stanford CIS-FMA program. Work was performed in part at the Stanford Nanofabrication Facility which is supported by the National Science Foundation through the NNIN under Grant No. ECS-9731293.

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